This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1.–23. (Cancelled)

24. (Previously presented) The structure of claim 45, further comprising:
a tensilely strained semiconductor layer disposed over the compressively strained layer.

25. (Previously presented) The structure of claim 45, wherein the compressively strained layer comprises a group IV element.

26. (Original) The structure of claim 25, wherein the compressively strained layer comprises at least one of silicon and germanium.

27 (Original) The structure of claim 26, wherein the strain of the compressively strained layer is greater than 1%.

28. (Previously presented) The structure of claim 45, wherein the compressively strained layer has a thickness of less than 500 Å.

29. (Original) The structure of claim 28, wherein the compressively strained layer has a thickness of less than 200 Å.

30. (Previously presented) The structure of claim 45, wherein the wavelength of the surface roughness is greater than 10 nanometers.

31. (Original) The structure of claim 24, wherein the tensilely strained layer comprises silicon.

32. (Previously presented) The structure of claim 45, wherein the compressively strained layer comprises at least one of a group III and a group V element.

33. (Original) The structure of claim 32, wherein the compressively strained layer comprises indium gallium arsenide.

34. (Original) The structure of claim 32, wherein the compressively strained layer comprises indium gallium phosphide.

35. (Original) The structure of claim 32, wherein the compressively strained layer comprises gallium arsenide.

36. (Previously presented) The structure of claim 45, wherein the compressively strained layer comprises at least one of a group II and a group VI element.

37. (Original) The structure of claim 36, wherein the compressively strained layer comprises zinc selenide.

38. (Original) The structure of claim 36, wherein the compressively strained layer comprises sulphur.

39. (Original) The structure of claim 36, wherein the compressively strained layer comprises cadmium telluride.

40. (Original) The structure of claim 36, wherein the compressively strained layer comprises mercury telluride.

41. (Previously presented) The structure of claim 45, further comprising:

a first transistor formed over the compressively strained layer, the first transistor including:

(i) a first gate dielectric portion disposed over a first portion of the compressively strained layer,

(ii) a first gate disposed over the first gate dielectric portion, the first gate comprising a first conducting layer, and

(iii) a first source and a first drain disposed proximate the first gate and extending into the compressively strained layer.

42. (Original) The structure of claim 41, wherein the first transistor is an n-type metal-oxide-semiconductor field-effect transistor and the first source and first drain comprise n-type dopants.

43. (Original) The structure of claim 41, wherein the first transistor is a p-type metal-oxide-semiconductor field-effect transistor and the first source and first drain comprise p-type dopants.

44. (Original) The structure of claim 41, further comprising:

a second transistor formed over the compressively strained layer, the second transistor including:

(i) a second gate dielectric portion disposed over a second portion of the compressively strained layer,

(ii) a second gate disposed over the second gate dielectric portion, the second gate comprising a second conducting layer, and

(iii) a second source and a second drain disposed proximate the second gate and extending into the compressively strained layer,

wherein the first transistor is an n-type metal-oxide-semiconductor field-effect transistor, the first source and first drain comprise n-type dopants, the second transistor is a p-type metal-oxide-semiconductor field-effect transistor, and the second source and second drain comprise p-type dopants.

45. (Previously presented) A structure comprising:

a compressively strained semiconductor layer having a strain greater than or equal to 0.25%,

wherein the compressively strained layer is substantially planar, having a surface roughness characterized by at least one of (i) an average roughness wavelength greater than an average wavelength of a carrier in the compressively strained layer and (ii) an average roughness height less than 10 nm.

46. (Previously presented) The structure of claim 45, further comprising:

a relaxed layer,

wherein the compressively strained layer is disposed over the relaxed layer.

47. (Previously presented) The structure of claim 26 wherein the compressively strained layer comprises a germanium content selected from a range of 0.4 to 0.6.

48. (New) A structure comprising:

at least a first transistor including:

(i) a first source and a first drain, the first source and first drain each comprising a compressively strained semiconductor having a strain greater than or equal to 0.25% and an average roughness height less than 10 nm, and

(ii) a first gate disposed over a strained semiconductor and between the first source and the first drain.

49. (New) The structure of claim 48, wherein the compressively strained semiconductor has a strain greater than 1%.

50. (New) The structure of claim 48, wherein the compressively strained semiconductor comprises $Si_{1-y}Ge_y$.

51. (New) The structure of claim 50, further comprising:

a relaxed $Si_{1-x}Ge_x$ region disposed proximate the compressively strained semiconductor, wherein y-x is equal to approximately 0.2.

52. (New) The structure of claim 48, wherein the first gate is disposed over a tensilely strained semiconductor.

53. (New) The structure of claim 48, wherein the strained semiconductor shares an interface with the compressively strained semiconductor.

54. (New) The structure of claim 48, wherein the strained semiconductor comprises silicon.

55. (New) The structure of claim 48, wherein the compressively strained semiconductor is disposed over a substrate, and a difference between a Ge content of the compressively strained semiconductor and a Ge content of the substrate is approximately 0.2.

56. (New) The structure of claim 48, wherein the first transistor is a p-type metal-oxide-semiconductor field-effect transistor and the first source and first drain comprise p-type dopants.

57. (New) The structure of claim 56, further comprising:

a second transistor including

(i) a second gate disposed over a tensilely strained semiconductor,

wherein the second transistor is an n-type metal-oxide-semiconductor field-effect transistor.